WEST Search History

DATE: Monday, November 24, 2003

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DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5 and l1	4	L6
L5	(instabilit$3 near5 (generat$3 or output$3))	2710	L5
L4	L3 and (instabilit$3 near5 (generat$3 or output$3))	1	L4
L3	L2 and l1	249	L3
L2	(375/$3.ccls. or 341/$4.ccls.)	66439	L2
L1	(delta near4 sigma$) and (feedback$) and (flip adj2 flop$)	396	L1

END OF SEARCH HISTORY

L6: Entry 3 of 4 File: USPT Sep 5, 1995

DOCUMENT-IDENTIFIER: US 5448202 A
TITLE: Sigma-delta FM demodulator

Parent Case Text (2):
The present application is a continuation-in-part of U.S. patent application Ser. No. 08/092,381, filed Jul. 14, 1993, now U.S. Pat. No. 5,345,188, and entitled SIGMA-DELTA DIGITAL FM DEMODULATOR.

Brief Summary Text (9):
In one preferred form of the present invention, the chosen transitions of the FM signal chosen for monitoring are all consecutive positive going transitions, i.e., consecutive rising edges in an associated intermediate frequency (IF) signal. The time differential between such chosen transitions provides a basis for inferring frequency of the FM signal. The anticipated transition times are taken from a set of two possible selections, an early selection and a late selection. The early selection is associated with a digital value "one" and the late selection is associated with a digital value "zero." For each selected anticipated time of transition, the associated digital value is reported, i.e., for each early selection a digital "one" is reported and for each late selection a digital "zero" is reported. The early selection is slightly less than the earliest next valid chosen transition and the late selection is slightly greater than the latest next valid chosen transition in the FM signal. Thus, choosing the early anticipated transition time always produces a negative error, and choosing the late transition time always produces a positive error. The accumulated error is the summation of all past errors, i.e., past differences between the actual times of the chosen transition and the selected anticipated times. Choosing the early anticipated time whenever the accumulated error is greater than zero and choosing the late anticipated time otherwise establishes negative feedback and assures an accumulated error value within given limits. The frequency of the signal is inferred from the ratio of reported "ones" to the total number of reported "ones" and "zeros."

Drawing Description Text (3):
FIG. 1 is a block diagram of a sigma-delta digital FM demodulator according to the present invention.

Drawing Description Text (4):
FIG. 2 is a timing diagram illustrating operation of the sigma-delta digital FM demodulator of FIG. 1.

Drawing Description Text (5):
FIG. 3 is a block diagram of an FM radio signal receiving device including a sigma-delta digital FM demodulator in accordance with the present invention.

Drawing Description Text (7):
FIGS. 5 and 6 are timing diagrams illustrating operation of the sigma-delta FM digital demodulator of the present invention.

Detailed Description Text (3):
FIG. 1 illustrates in block form the general arrangement of a sigma-delta digital FM demodulator according to the present invention. FIG. 2 is a timing diagram illustrating an FM signal processed by the demodulator of FIG. 1 and various signals developed by the demodulator of FIG. 1 during demodulation in accordance with the present invention.

Detailed Description Text (4):

In FIGS. 1 and 2, sigma-delta FM digital demodulator 10 receives a limited FM signal 12 and provides a digital output 14. FM signal 12 is a limited FM signal, i.e., a square wave, having amplitude variation between, for example, negative one and positive one volt. Transitions in the FM signal 12 represent frequency of the FM signal 12. For example, FM signal 12 can be derived from an FM radio signal broadcast and converted to an intermediate frequency (IF) signal for demodulation as is typically done in conventional FM radio signal processing. As explained more fully hereafter, digital output 14 represents the frequency of FM signal 12, the frequency information being later recovered by further analysis of digital output 14.

Detailed Description Text (10):
Application of the multiplier output 17 to an integrator 30 generates representation of errors in the anticipated next transition 21 relative to the actual next transition 28, and further accumulates such errors over time. For example, if the time of the anticipated next transition 21 were exactly correct, integrator 30 integrates a negative one volt signal for the same period of time it integrates a positive one volt signal with a net accumulation of no error, i.e., delta S difference 37 equals zero. As the anticipated next transition 21 deviates from the actual next transition 28, however, integrator 30 integrates one of a positive or a negative voltage for a relatively greater time and thereby accounts for the error in the anticipated transition 21, i.e., measures the time differential 29. Integrator 30 continuously integrates the multiplier output 17 throughout operation of the demodulator 10. By selecting each anticipated next transition 21 under negative feedback, the integrator output 35, also designated S, remains within a given range.

Detailed Description Text (12):
The integrator output 35, i.e., the overall accumulated error in time of anticipated transitions 21 relative to time of corresponding actual transitions 28, is applied to an analog-to-digital block 32. Analog-to-digital block output, also designated Y, is the digital output 14. By applying the digital output 14 to the address input 20a of multiplexer 20, the accumulated error, i.e., the integrator 30 output 35, is maintained within a given range by negative feedback. As the accumulated error moves in a given direction, the multiplexer 30 appropriately selects one of the trigger signals 22 to move when necessary the accumulated error in the opposite direction. Overall, the accumulated error represented in the integrator output 14 remains within a given range as a result of such negative feedback.

Detailed Description Text (14):
Center frequency control signal 25 and frequency deviation control signal 23 operate dynamically to maintain appropriate adjustment in the delay elements 24 and 26. More particularly, upon start up the frequency deviation control signal 23 is set to maximum delay and the center frequency control signal 25 is set to a mid-point delay. A negative feedback loop is then executed to adjust the center frequency control signal 25 until the digital output 14 averages one half of N-1. Overall, it is assumed that the average occurrence for actual next transitions 28 is the center of the window of valid next transitions in FM signal 12. Based on this assumption, adjusting center frequency control signal 25 until the digital output averages one half of N-1 insures that the group of available anticipated transition times are well centered about the window of valid next transitions in the FM signal 12. This negative feedback control loop for the center frequency control signal 25 remains in operation during use of the sigma-delta digital FM demodulator 10.

Detailed Description Text (16):
The above described FM demodulator 10 is set forth in general terms and could be implemented in a large scale digital circuit wherein the digital output 14 is at a given resolution, i.e., number of bits in each value presented, and a given size of multiplexer 20, i.e., selection among a large number of possible trigger signals 22 very closely spaced in time. As may be appreciated, the greater the resolution in digital output 14 and the larger the number of trigger signals 22 the more accurate the FM demodulation. Greater processing overhead, circuit resources and component tolerances are required for such accuracy and resolution. The invention can be implemented, however, on a much smaller scale while still providing meaningful frequency information. For example, small scale A-to-D conversion, e.g., 2-bit flash

convertors, may be used in a relatively small scale implementation of the present invention. Thus, while the sigma-delta FM demodulator described herein can be implemented at higher resolution and complexity, such implementations may be of considerable size and may not be justified in light of alternative FM demodulation methods and devices available. For smaller scale implementations, however, the FM demodulator of the present invention can be an effective solution to FM demodulation in a miniaturized FM signal receiver.

Detailed Description Text (19):
The FM radio signal 112 is first processed by the radio receiving device 110 in an intermediate frequency (IF) generator 118. Generator 118 corresponds to a conventional FM receiver up to, but not including, the discriminator circuit. As will be appreciated by those skilled in the art, IF signal 120 is a square wave signal corresponding in frequency to that of the FM radio signal 112, but mixed to the intermediate frequency and amplified until limiting occurs, thereby producing a signal with two amplitude values and transitions occurring at a fairly uniform rate according to signal frequency. Thus, the frequency of IF signal 120 is a function of the frequency of the FM radio signal 112, and provides a basis for FM demodulation. The IF signal 120 produced by IF generator 118 is applied to a sigma-delta digital FM demodulator 122 of the present invention.

Detailed Description Text (20):
The sigma-delta FM digital demodulator 122, described in more detail hereafter, produces a signal 120 frequency dependent, i.e., non-uniform, sample or bit clock signal 124 and a bit stream 126. The bit stream 126 provides a sequence of logic values, i.e., ones and zeros, and the sample clock 124 provides a basis for sampling values from the bit stream 126. A non-uniform decimator block 128 receives the non-uniform clock 124 and bit stream 126 and, based on the proportion of ones and zeros in bit stream 126, provides frequency data 130 to a data recovery block 132 upon activation of a uniform frequency collect signal 134. Data recovery block 132 uses conventional uniform sampling according to known digital signal processing (DSP) techniques to filter and recover a pager data stream 138 and a pager bit clock 139. A use block 136, which constitutes the bulk of the radio receiving device 110, interprets the pager data 138 and pager data bit clock 139 according to a given data protocol, and displays the paging messages according to a given user interface.

Detailed Description Text (33):
FIG. 6 illustrates various signals developed in the sigma-delta FM digital demodulator 122 for a given condition of the IF signal 120. In FIG. 6, the IF signal 120 presents a frequency wherein the next actual transition 202 (FIG. 5) occurs at a point two-thirds into the window of valid next transitions, i.e., two-thirds of the way from the time t.sub.1 to the time t.sub.0. Four cycles of circuit 122 operation are illustrated in FIG. 6. In the first cycle, the integrator output 152 is negative and the late gate G0 is selected for presentation in the signal 143 to the switch 144. The integrator output 152 then increases toward positive, but does not yet pass zero. Because the integrator output 152 is negative in this next cycle, the late gate G0 is again selected for application to the switch 144. In response, the integrator output 152 again moves in the positive direction, but this time passes zero and presents a positive voltage to comparator 154. In this next cycle, therefore, the early gate G1 is selected for application to the switch 144 and, in response thereto, the integrator output 152 moves in the negative direction.

Detailed Description Text (42):
FIG. 8 illustrates various timing relationships between the signals of the circuit of FIG. 7 and should support, for one skilled in the art, implementation of the synchronizer 130. The synchronized sample request 135 is a signal generated by cascading two type D flip-flops clocked by non-uniform bit clock 127 and receiving as input the sample request 134. The variable M in FIG. 8 refers to the six bit value 301 taken from the samples register 300. The variable P refers to the six bit value 307 taken from the ones counter 306. As previously noted, the values M and P are joined to form an address applied to the look up table 313. The data stored in the corresponding address should represent a division of the variable P by the variable M. Such data could further include any correction factors considered necessary relative to circuit characteristics and especially those required to correct for the higher order terms of the power series mentioned earlier.

Detailed Description Text (43):
FIG. 9 is a simplified diagram illustrating an alternative embodiment of the present invention avoiding use of an analog device, e.g., an integrator, to represent an accumulated error in the sigma-delta FM demodulator. The illustration of FIG. 9 is not presented as an implementation design, but rather to illustrate the theory of operation for this embodiment of the present invention. FIGS. 10 and 11 illustrate implementation details for this form of the invention.

Detailed Description Text (50):
The choice between the lesser magnitude and greater magnitude frequency of operation for oscillator 401 is a function of the Q output 470c of latch 470. The Q output 470c of latch 470 represents the relative timing, i.e., early or late, of the pulse 454 at the oscillator output 453 relative to a transition of interest in the FM signal 411. Valid frequencies in the FM signal 411 are assumed to be between the greater magnitude frequency represented by short delay block 414 and the lesser magnitude frequency represented by the long delay block 412. The digital demodulator of FIG. 9 selects between two frequencies, i.e., two delay paths within oscillator 401, through negative feedback. The average frequency of operation for oscillator 401 may be taken as a weighted average of the greater magnitude frequency and the lesser magnitude frequency, i.e., a frequency somewhere between the lesser magnitude frequency associated with the long delay block 412 and the greater magnitude frequency associated with the short delay block 414.

Detailed Description Text (54):
By selecting the frequency of oscillator 401 during the next cycle with negative feedback from the current cycle, it can be assumed that at the end of the next cycle pulse 454 arrival at clock input 470d moves toward the next FM signal 411 transition arrival at D input 470a. The demodulator always moves toward and achieves a stable condition whereby pulse 454 is either retarded or advanced, i.e., by routing through the selected one of delay blocks 412 and 414, relative to the next occurrence of the FM signal 411 transition of interest. If the FM signal 411 transition occurs before the pulse 454, then the latch 470 receives at its D input 470a a value one when it is clocked by pulse 454. If the FM signal 411 transition occurs after the pulse 454, then the latch 470 receives at its D input 470a a value zero when it is clocked by pulse 454.

Detailed Description Text (56):
Accordingly, depending on whether the circulating pulse 454 is ahead or behind an FM signal 411 transition of interest, the appropriate one of delay blocks 412 and 414 is selected to move the next pulse 454 toward the next FM signal 411 transition of interest. Eventually, a late circulating pulse 454 becomes an early pulse 454 and an early pulse 454 becomes a late pulse 454. In the next cycle of operation, the other delay block is selected to again move the next occurrence of pulse 454 toward the next FM signal 411 transition of interest, but in the opposite direction. Thus, switch 450 remains in a given state while the circulating pulse 454 moves toward the next FM signal 411 next transition of interest. Eventually the circulating pulse 454 moves past the next FM signal 411 transition of interest, and switch 450 changes state. Thus, the demodulator circuit of FIG. 9 operates in negative feedback fashion to maintain the occurrence of pulse 454 within a given proximity of the FM signal 411 transition of interest.

Detailed Description Text (61):
As described herein above, sigma-delta frequency demodulation under the present invention stores an accumulated error following each crude estimate of a next anticipated transition of interest. Each crude anticipated time of transition is accepted, but the magnitude of error is carefully and accurately accumulated whereby, in conjunction with negative feedback, the error is forced to be zero over an extended interval. In the earlier embodiments, such error was accumulated in an analog device, e.g., an analog integrator. Error accumulation represented by the demodulator of FIG. 9 corresponds to the position of pulse 454 within the oscillator 401. This may be viewed as an analog storage of error, but an analog device need not be used in implementation of delay blocks 412 and 414. In an actual implementation by integrated circuit, the "position" of pulse 454 corresponds to the position of state transition within a series of gate delays.

Detailed Description Text (62):
Thus, the sigma-delta FM demodulator of the present invention may be improved by eliminating the use of an analog device, e.g., analog integrator, to store an accumulated measure of error in selected anticipated times of next FM signal transition. Under such improvement, one need not store an analog measurable quantity, but rather may advantageously represent error in an analog fashion by virtue of a position along a digital delay element. Thus, it is not the voltage of a pulse or the length of a pulse which stores accumulated error, but rather the position of a pulse within a digital delay line.

Detailed Description Text (70):
Thus, one use of clock 553, i.e., the pulse 554 as presented by multiplexor 550, is to avoid passing any metastable oscillations of latch 570 onto demodulator output data 578. While the additional latch 576 does introduce an additional delay in data 578 presentation, it avoids instability on the data output 578.

Detailed Description Text (76):
The positive-going transition demodulator circuit 701 includes a switch 750 comprising the gates 750a, 750b, and 750c of similar arrangement to the multiplexor 550 of FIG. 10. Demodulator circuit 701 further includes latches 770 and 776 corresponding to the latches 570 and 576 of FIG. 10. Similarly, demodulator circuit 703 includes a switch 760 comprising gates 760a, 760b, and 760c corresponding to the multiplexor 550 of FIG. 10 and a pair of latches 780 and 786 corresponding to the latches 570 and 576 of FIG. 10. Circuit 701 and 703 operate alternately as RS flip-flop 751 alternately enables the switches 750 and 760.

Detailed Description Text (77):
RS flip-flop 751 includes a pair of NOR gates 756 and 766 each receiving at a first input thereof a corresponding one of the switch 750 and 760 outputs. A second input of each of NOR gates 756 and 766 receives an initialize signal 714, the initialize signal 714 being applied directly to the NOR gate 756 and indirectly to the NOR gate 766 by way of a pair of inverters 716a and 716b. The output of NOR gate 756 applies to a third input to NOR gate 766 and the output of NOR gate 766 applies to a third input of NOR gate 756.

Detailed Description Text (81):
The delay controls 700a and 700b of major delay element 700 are provided as an automatic center frequency control mechanism. As discussed herein above, by observing the data provided by the demodulator circuit, i.e., data P output 778 and data N output 788, a long term average may be established for these values and forced to zero by using negative feedback on the controls 700a and 700b. For example, if over an extended period more values one are found in the data output than values zero, then the delay element 700 will be altered (made shorter) to favor more values zero. Thus, the major delay controls 700a and 700b may be operated dynamically to control the positive-going transition delay and negative-going transition delay, respectively. Delay controls 702a and 704a for the delay elements 702 and 704, respectively, operate to set the gain of the demodulator circuits. In other words, to control the frequency deviation or extent of frequency excursion permitted in the FM signal 411. These controls are set through methods similar to that described above wherein circuit output of the decimator is forced to a certain excursion range, e.g. 3/4 full scale, over a long period of time. If the range of the output signal is less than 3/4 scale, then controls 702a and 704a are adjusted such that the delays move closer together which will cause smaller delay difference between 702 and 704 and thereby cause a wider range of one values and zero values in the circuit output for similar deviations in FM signal 411. Similarly, if the frequency range excursion begins to exceed 3/4 scale, e.g., becomes all ones or all zeros for an extended time indicating that the FM signal is at a frequency outside the range allotted by the difference between delay provided in elements 702 and 704, then controls 702a and 704a are increased. This lowers the gain of the FM signal demodulator and brings the signal within the frequency range of the demodulator as established by the delay elements 702 and 704.

Detailed Description Text (84):
No pulse generator is required because the circuit triggers in response to positive

and negative transitions cycling through the circuit. Thus, as the FM signal 411 presents alternating positive-going and negative-going transitions, with every positive-going transition the demodulator circuit 701 operates to select a shorter or longer delay at switch 750 for the positive-going transition emerging from the delay network 705. For each negative-going transition, the same occurs at switch 760 in demodulator circuit 703 for negative transitions emerging from delay network 705. RS flip-flop 751 toggles between the positive transition mode and the negative transition mode. The RS flip-flop 751 reflects which of the demodulator circuits 701 and 703 are enabled and drives the switches 750 and 760.

Detailed Description Text (88):
FM signal 411 demodulation begins when the initialize signal 714 is removed, i.e., taken low. Delay gates 716a and 716b delay this transition in the initialize signal 714 relative to the input of gate 766. This causes an initial condition in the RS flip-flop 751 where the output of gate 766 remains low and the output of gate 756 transitions to high. This ensures that when the initialize signal 714 goes low, the output of gate 756 will go high. This important transition drives the circuit into operation. The output of gate 756, being driven immediately high, will arrive at the input of gate 766 before the output of the delay gate 716b goes low. Accordingly, gate 766 will not change state and its output will remain low until later when events ripple through the circuit as described hereafter.

Detailed Description Text (91):
Concurrently with presentation to the latch 770, the rising edge in clock 754 also arrives as an input to the gate 756. This condition causes the output of gate 756 to go low and the output of gate 766 to go high. Accordingly, the RS flip-flop 751 has changed state. The negative transition of gate 756 as presented on signal line 758 enters major delay element 700 and later enters in parallel long and short delay elements 702 and 704 as a negative transition. Because gates 750a and 750b are now disabled, as a result of the signal line 758 being low, the negative-going transition does not enter circuit 701, but rather travels down through the inverters 710 and 712 to circuit 703 and appears as, a positive-going edge. This rising edge then enters gates 760a and 760b of switch 760, then enabled by virtue of the high state on signal line 768. Depending on the state of switch 760, a selected one of the gates 760a and 760b passes this rising edge to OR gate 760c for presentation as a clock 764 to the latch 780. This clocks the latch 780 and indicates, as described herein above, the relative timing of the clock signal rising edge at the latch 780 relative to the negative-going transition in the FM signal 411, which appears inverted as a positive-going transition in signal 411a.

Detailed Description Text (92):
In addition to clocking the latch 780, the rising edge transition presented by clock 764 also applies to the RS flip-flop 751. In particular, the rising edge applies to an input of the gate 766. This causes gate 766 output to go low and thereby causes the output of gate 756 to go high. This returns the circuit to the initial state described above and the circuit continues to iterate between operation of the demodulator circuit 701 and demodulator circuit 703. Thus, a circulating edge travels through the demodulator of FIG. 11 causing alternating enabling and disabling conditions, by way of the RS flip-flop 751, in the switches 750 and 760 of the demodulator circuits 701 and 703, respectively, and generating alternating clocks 754 and 764 which cause latches 770 and 780 to alternately sample FM signal 411 for the positive and negative transitions.

Detailed Description Text (93):
Because the demodulator circuit is self-correcting by negative feedback and will always bring the circulating edge transition within a given proximity of the FM signal 411 transitions, the initialize signal 714 may be removed arbitrarily at any time. However, the circuit may be brought more quickly into demodulation by synchronizing removal of the initialize signal 714 in relation to the FM signal 411 transitions of interest. In other words, remove the initialize signal 714 at a time when the circulating edge transition will occur close to the next FM signal 411 transition of interest. In this manner, the demodulator circuit will more quickly begin providing meaningful output, and therefore more quickly begin presenting information sufficient to derive frequency of the FM signal 411.

Detailed Description Text (95):
For example, the sigma-delta digital FM demodulator of the present invention bears some similarity to sigma-delta analog-to-digital data convertors. Many enhancements have been developed with respect to such sigma-delta analog to digital convertors, and these enhancements can be applied to the sigma-delta FM digital demodulator of the present invention. Such enhancements include an integrator having more than one pole, i.e., a multi-pole integrator or integrators in combination with band pass filters having poles at non-zero frequencies. Such a multi-pole combination can force quantization noise away from data frequencies and thereby provide enhanced signal processing. After having the benefit of the present disclosure, and familiarity with sigma-delta analog-to-digital convertors, those skilled in the art will appreciate that other enhancements applicable to sigma-delta analog-to-digital convertors may be equally applicable to design modifications of sigma-delta digital FM demodulators in accordance with the present invention.

Other Reference Publication (1):
Two articles entitled "A Use of Limit Cycle Oscillations to Obtain Robust Analog-to-Digital Converts" and Table-Based Simulation of Delta-Sigma Modulators. Both articles are located in a manual entitled Oversampling Delta-Sigma Data Converters published by The Institute of Electrical and Electronics Engineers, Inc. in 1992.

WEST Search History

DATE: Monday, November 24, 2003

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L13	(375/247.ccls. or 375/242.ccls. or 341/143.ccls. or 341/77.ccls.)	2583	L13
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L2	(delta near3 sigma near3 2$modulat$3) and ((cascad$3 or serial$3 or series$3) near4 (flip adj flop$))	0	L2
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END OF SEARCH HISTORY